## REMARKS

In a Final Office Action dated February 20, 2009, the Examiner maintained the previous rejection of Claims 1-2 and 11-12 under 35 USC §103(a) as being unpatentable over U.S. Patent No.7,111,303 issued to Macchiano et al. ("Macchiano"). The Examiner has also maintained the previous rejection of Claims 3-10, 13-20 and 31-61 under 35 USC §103(a) as being unpatentable over Macchiano in view of Applicant's Admitted Prior Art ("AAPA").

In this response, Applicant respectfully traverses the rejections. No amendments are presented. Applicant requests reconsideration of Claims 1-20 and 31-61 in view of arguments as set forth in detail in the following remarks.

**CLAIM 1-2, AND 11-12 REJECTIONS – 35 U.S.C. § 103**

Claims 1-2, and 11-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Macchiano. Applicant traverses the rejection.

In making this rejection, the Examiner is attempting to base his argument of obviousness on a modification of a single reference, namely the modification of the Macchiano reference. As before, the Examiner concedes that Macchiano does not explicitly teach the use of a shared physical memory element (Office Action dated 2/20/2009, Page 3, Para no. 5). The Examiner argues, however, that "Macchiano does teach the use of internal buffer storage for data transfers on the virtual LAN," and concludes that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention that internal buffer storage is in fact a shared physical memory element." (Office Action dated 2/20/2009, Page 3, Para no. 5, citing Macchiano, Col. 5, Lines 23-25).

By way of further explanation, the Examiner now argues that [t]he internal buffer storage of Macchiano is used to facilitate transfers between virtual NICs operating on the virtual LAN. Since any virtual NIC is permitted to use this internal buffer storage, this storage (i.e. memory) is shared amongst the virtual NICs. As such, the Examiner reasons, Macchiano's internal buffer storage can be interpreted to be a shared physical memory element. (Final Office Action, 2/20/2009, Page 19.)

Thus, while the Examiner previously asserted that "the internal buffer storage *is in fact* a shared physical memory element," (emphasis added), the Examiner now retreats from that position, and instead argues that the internal buffer storage can be *interpreted to be* a shared physical memory element. Applicant again disagrees, and submits that the Examiner's conclusion is, at best, an impermissible hindsight influenced by knowledge of the Applicant's disclosure, and is not properly based on the prior art.

For at least the above reasons, Applicant submits that the Examiner has failed to establish a *prima facie* case of obviousness. As noted in the Manual of Patent Examining Procedure ("MPEP"), [t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed.

Cir. 2006). See also KSR, 550 U.S. at ___ , 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). MPEP §2142 Legal Concept of *Prima Facie* Obviousness.

For at least these reasons, applicant respectfully requests that the Examiner withdraw the rejection of Claims 1-2 and 11-12.

**CLAIM 3-10, 13-20, 31-61 REJECTIONS – 35 U.S.C. § 103**

Claims 3-10, 13-20 and 31-61 were rejected as being unpatentable over Macchiano in view of Applicant Admitted Prior Art ("AAPA"). The rejection is based on the same rationale as the rejections of Claims 1-2 and 11-12 – namely, that the internal buffer storage of Macchiano is, in fact, a shared physical memory element. However, as already noted, there is nothing in Macchiano that indicates that the internal buffer storage is a shared physical memory element, and the remaining disclosure in the AAPA does not cure this deficiency in Macchiano. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of Claims 2-10, 13-20 and 31-61 for at least this reason.

With regard to the arguments in support of the rejection of Claims 41-47, Applicant again observes that the Examiner is equating the virtual LAN disclosed in Macchiano with the first direct memory access (DMA) buffer recited in the claims. The Examiner had previously argued "the virtual LAN is *equivalent* to a direct memory access buffer in that it acts as a medium to allow the sending and retrieval of transmitted data." (Office Action dated 7/31/2008, Page 12, Para No. 39). Now, the Examiner argues that the use of direct memory access buffers is taught by Macchiano because the direct memory access buffer *is equivalent to* the internal buffer storage. (Office Action dated 2/20/2009, Page 21) Applicant disagrees.

First, the virtual LAN of Macchiano, at best, employs internal buffers, but it is not a buffer itself. Moreover, there is nothing in Macchiano to suggest that the internal buffer storage used in the virtual LAN is made up of direct memory accessible storage. Thus, it is incorrect to say that the use of direct memory access buffers is taught by Macchiano. The most that can be said of Macchiano is that it teaches the use of internal buffer storage in virtual LANs. Accordingly, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47 for at least this reason.

Lastly, as noted in Applicant's previous response, in the instant application, the description of Fig.1 and elsewhere in the specification makes a clear distinction between *separate* physical memory elements 181 and 182 as illustrated in Fig. 1, and a *shared* physical memory element. Thus, there is nothing that would support an argument that the *separate* physical memory elements 181 and 182 as illustrated in Fig. 1, disclose the direct memory access buffers recited in the claims. In response, the Examiner now argues that the *separate* physical memory elements 181 and 182 were only used in the rejection of Claim 41 "for teaching that the mapping of a transmitting buffer and mapping buffers for data transfers in both directions are known." (Final Office Action, 2/20/2009, Page 21). But this response still does not address the failure of either the AAPA or Macchiano to disclose the use of direct memory access buffers as recited in Claim 41. For at least this reason, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47.

## CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, Claims 1-20 and 31-61 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application. Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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April 20, 2009
Date

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